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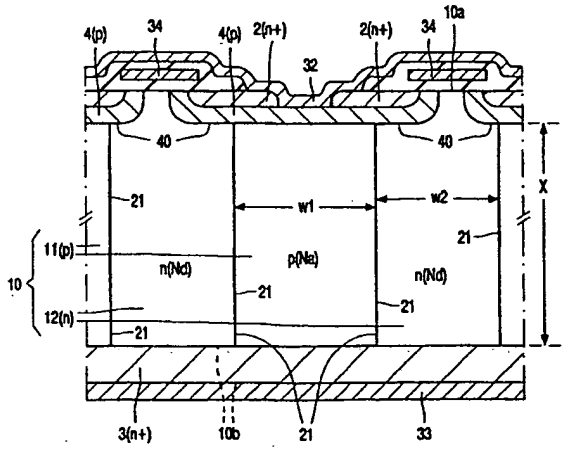
(54) Title: METHOD OF MAKING A CHARGE COMPENSATION SEMICONDUCTOR DEVICE USING DIRECT BONDING AND CORRESPONDING DEVICE



(57) Abstract: Semiconductor devices such as high voltage MOSFETA are known comprising a depletable multiple-region semiconductor material (10) with alternating p-type (11) and n-type (12) regions that provides a voltage-sustaining space-charge zone when depleted from a blocking junction (40). The invention provides a low-cost yet reliable way of manufacturing such a material (10) wherein the depletable multiple-region semiconductor material is produced by directly bonding alternate p-type and n-type wafers (110, 120) to each other at optically-flat major surfaces. The resulting material is in the form of a bonded stack having bonded junctions (21) between the p-type and n-type regions (11, 12). The bonded junctions (21) may be p-n junctions or may comprise an oxide interface layer. The bonded stack may be sliced transverse to the junctions (21) to form a device wafer for a vertical device.

WO 01/06550 A1

DESCRIPTION

METHOD OF MAKING A CHARGE COMPENSATION SEMICONDUCTOR DEVICE USING DIRECT BONDING AND CORRESPONDING DEVICE

This invention relates to the manufacture of semiconductor devices with a depletable multiple-region semiconductor material that provides a voltage-sustaining space-charge zone when depleted, and to a method of fabricating such a material. The invention also relates to semiconductor material and semiconductor devices produced by such methods.

The voltage-sustaining space-charge zone results from charge-carrier depletion of interposed p-type and n-type regions. The intermediate dimensions (width or thickness) of the interposed p-type and n-type regions need to be small enough (in relation to their dopant concentrations) to allow depletion of the region across its intermediate dimension without the resulting electric field reaching the critical field strength at which avalanche breakdown would occur in that semiconductor. This is an extension of the famous RESURF principle. Thus, the depletable multiple-region material may be termed "multiple RESURF" material. In the voltage-sustaining zone formed of first regions of one conductivity type interposed with second regions of the opposite conductivity type, the dopant concentration and dimensions of the first and second regions are such that (when depleted in a high voltage mode of operation) the space charge per unit area in the first and second regions balances at least to the extent that the electric field resulting from the space charge is less than the critical field strength at which avalanche breakdown would occur in that zone.

United States patent specification US-A-4,754,310 (our ref: PHB32740) discloses semiconductor devices with depletable multiple-region (multiple RESURF) semiconductor material comprising alternating p-type and n-type regions which together provide a voltage-sustaining space-charge zone when depleted. The use of such material for the space-charge zone permits the achievement of a lower on-resistance in the device having a given breakdown

voltage and is particularly advantageous for high voltage MOSFET devices, both lateral devices and vertical devices. Other embodiments of such devices are disclosed in United States patent specification US-A-5,438,215 and WO-A-97/29518. The whole contents of US-A-4,754,310, US-A-5,438,215 and WO-A-97/29518 are hereby incorporated herein as reference material.

As described in US-A-4,754,310, US-A-5,438,215 and WO-A-97/29518, epitaxial refill of etched trenches may be used to provide the alternating p-type and n-type regions extending perpendicular to the major surface of the device body in the case of a vertical device. However, the quality of the resulting junctions and the reproducibility of the process is far from optimum. Figures 7a to 7b of WO-A-97/29518 suggest using repeated epitaxy with ion implantation of the opposite type dopant at each epitaxial stage. However this process involves many steps and so is expensive, and it is difficult to achieve the balance of the n and p dopant concentrations that is needed for depletion, together with the conductivity and voltage blocking requirements of the device. Due to the closely matched p and n type doping in cm^{-2} that is needed for the multiple RESURF, it is not obvious what known processes could be advantageously used in manufacture to fabricate the depletable multiple-region (multiple RESURF) semiconductor material for vertical devices.

It is an aim of the present invention to provide a low-cost yet reliable process for fabricating depletable multiple-region (multiple RESURF) semiconductor material.

According to the present invention, there is provided a method of fabricating a depletable multiple-region (multiple RESURF) semiconductor material comprising alternating p-type and n-type regions which provide a voltage-sustaining space-charge zone when depleted, by directly bonding alternate p-type and n-type wafers to each other at optically-flat major surfaces to provide the multiple-region semiconductor material in the form of a bonded stack having bonded junctions between the p-type and n-type regions.

The bonded junctions may be p-n junctions between the alternate wafers. Alternatively, they may comprise an insulating interface layer, for

example of silicon dioxide when the wafers are of silicon. Such an interface layer can be formed on the major surfaces of at least alternate wafers before the direct bonding step.

These and other advantageous technical features in accordance with the present invention are set out in the appended Claims. They are illustrated in embodiments now described, by way of example, with reference to the accompanying diagrammatic drawings, in which:

Figure 1 is a cross-sectional view of part of a high voltage MOSFET device manufactured in accordance with the invention;

Figure 2 is a cross-sectional view of a plurality of wafers of alternate conductivity types before being directly bonded to form a depletable multiple-region (multiple RESURF) material for the device of Figure 1;

Figure 3 is a cross-sectional view of a bonded stack of the wafers of Figure 2 before being sawn into device wafers; and

Figures 4a and 4b are enlarged views of part of the Figure 3 stack, showing alternative forms of bonded junctions.

It should be noted that the Figures are diagrammatic, relative dimensions and proportions of parts of the drawings having been shown exaggerated or reduced in size, for the sake of clarity and convenience in the drawings. Thus, for example, the thickness X of the portion 10 is typically at least an order of magnitude larger than the widths w1 and w2 of its regions. The same reference signs are generally used to refer to corresponding or similar features in modified and different embodiments.

The MOSFET device of Figure 1 includes a monocrystalline silicon body having a body portion 10 of a depletable multiple-region (multiple RESURF) semiconductor material that comprises alternating p-type and n-type regions 11 and 12 respectively. The regions 11 and 12 together provide a voltage-sustaining space-charge zone when depleted in a blocking state of the MOSFET. This device is of the kind disclosed in US-A-4,754,310,

US-A-5,438,215 and WO-A-97/29518. Typically the multiple RESURF semiconductor material may sustain blocking voltages in excess of 100 volts.

The MOSFET of Figure 1 is a vertical device having source and drain regions 2 and 3 respectively, that are provided adjacent to opposite major faces 10a and 10b of the body portion 10. The insulated gate structure 34 and source electrode 32 of the MOSFET are present at the face 10a, while the drain electrode 33 is present at the face 10b. The junctions 21 between the regions 11 and 12 extend transverse to the major surfaces 10a,10b of the body portion 10. The source region 2 is separated from the multiple junctions 21 of the space-charge zone by a channel-accommodating body region 4. This transistor body region 4 is of opposite conductivity type to the drain region 3 and forms the blocking p-n junction 40 from which the depletion layer spreads in the body portion 10 in the blocking state of the MOSFET. When sustaining the blocking voltage, the whole of the body portion 10 is depleted and so is shown unhatched in Figure 1. The depletion layer also extends slightly from the body portion 10 into the regions 3 and 4.

A method of fabricating the body portion 10 of this device by a method in accordance with the present invention will now be described. This method includes the steps of:

(a) providing a plurality of semiconductor wafers 110 of p-type conductivity and a plurality of semiconductor wafers 120 of n-type conductivity each having optically flat major surfaces 100a and 100b, the wafers 110 and 120 comprising respective doping concentrations Na, Nd for the regions 11 and 12 of the depletable multiple-region (multiple RESURF) material and having respective thicknesses t1 and t2 between their major surfaces that correspond to a desired dimension w1 and w2 for the regions 11 and 12, and

(b) directly bonding alternate p-type and n-type wafers 110 and 120 to each other at their major surfaces 100a and 100b to provide the depletable multiple-region (multiple RESURF) semiconductor material in the form of a bonded stack 100 having bonded junctions 21 between the p-type and n-type regions 11 and 12.

The direct bonding of semiconductor wafers is a known process, for example as described in the Philips Journal of Research Vol.49 No.1/2 1995, a special issue on direct bonding. In particular reference is invited to the two papers on pages 47 to 89: "Surface-related phenomena in the direct bonding of silicon and fused-silica wafer pairs" by G.A.C.M. Spierings et al., and "Silicon-wafer fabrication and (potential) applications of direct-bonded silicon" by J. Haisma et al. The whole contents of these two papers are hereby incorporated herein. The major surfaces of the wafers to be bonded are polished so as to be optically flat with a surface roughness of less than 50nm (nanometres) and preferably less than 5nm. When these optically flat surfaces are brought into contact, they bond together by attractive Van der Waals forces. The bonded wafers are then usually subjected to a heat treatment to strengthen the bond. The present invention relates to a new use of direct bonding, not previously envisaged.

In accordance with the present invention, the thickness t1, t2 and doping concentration Na, Nd of the separate wafers 110 and 120 are chosen to give the necessary space-charge balance in cm^{-2} between the regions 11,12 when depleted. Typically, the wafers are of monocrystalline silicon. Thus, the space charge per unit area (Na.w1) and (Nd.w2) provided by each of these silicon wafers 110 and 120 must be effectively matched, i.e. balanced to the extent that an electric field resulting from any imbalance is less than the critical field strength at which avalanche breakdown would occur in the silicon semiconductor material.

The starting material may be two ingots of uniformly doped monocrystalline silicon of almost equal doping level Na and Nd, one p-type and the other n-type. These two ingots may be sawn and polished into the thin wafers 110 and 120, for example, each with a thickness of less than 20 μm (micrometres). These wafers 110 and 120 are then stacked alternately as in Figure 1, and brought into contact to form the bonded stack 100 of Figure 2. The stack is then heat treated, for example in the temperature range of 900°C to 1200°C. The resulting strongly-bonded stack 100 may be subsequently sliced transverse to the bonded junctions 21 of the p-type and n-type wafers

(for example, as indicated by the line 200 in Figure 2) to provide semiconductor slices 210 whose major surfaces are subsequently polished to provide thin wafers for device manufacture. Thus, the bonded stack 100 may be sawn at right angles to the wafers 110 and 120 to produce the device wafers 210 with vertical n and p regions 11 and 12. This wafer 120 may then be provided with electrodes 32 and 33 for defining through the material a current path that extends parallel to the bonded junctions 21 and transverse to major surfaces of the wafer 120.

Thus, the resulting polished wafers 210 with their alternating regions 11 and 12 may be further processed in known manner to form the MOSFET of Figure 1, by providing the drain region 3 at one major surface and the source and body regions 2 and 4 at the opposite major surface. In the case of an n-channel device, the region 4 is p-type, and the substrate 3 is highly doped n-type. In the case of a p-channel device, the region 4 is n-type and the substrate 3 is highly doped p-type.

The regions 2, 3, and 4 may be formed by dopant implantation and diffusion into the wafer 210. However, long diffusion times cannot be used without also diffusing the doping concentrations Na and Nd of the multiple RESURF regions 11 and 12. Thus, if a thicker drain region 3 is desired, then an appropriately doped n-type wafer may be directly-bonded to the face 10b of the wafer 210 to provide the drain region 3. Thus, depending on how the region 3 is provided, the major face 10b of the body portion 10 may be the bottom surface of the device body or the interface with the region 3. In order to illustrate both of these alternatives, the reference 10b is shown with two dashed lead-lines in Figure 1.

In some devices, it may not be necessary to align the source region 2 and channel-accommodating body region 4 with respect to the p-type and n-type regions 11 and 12 at the major face 10a of the body portion 10. This can be the case when the regions 2 and 4 have a longitudinal layout that is orientated transverse to a longitudinal layout of the regions 11 and 12 and/or when using a very large number of very narrow regions 11 and 12.

In other devices, for example with a close-packed hexagonal or square cellular layout for the regions 2 and 4, it may be desirable to align the regions 2 and 4 with respect to the regions 11 and 12. In this case, it is necessary to identify the locations of the p-type and n-type regions 11 and 12 at the major face 10a before providing the source region 2 and channel-accommodating body region 4 adjacent the major face 10a.

This location identification can be achieved in a variety of ways. Lightly etching the face 10a in a selective etchant is a particularly convenient means of revealing the locations of the p-type and n-type regions 11 and 12 at face 10a. The etchant may be such as to etch preferentially p-type conductivity material. Having identified the locations of the p-type and n-type regions 11 and 12 at the face 10a, the insulated gate 34 may then be aligned with respect to the p-type and n-type regions 11 and 12 at said one major face 10a and may act subsequently as an implantation mask for providing the source region 2 and the channel-accommodating body region 4.

The thickness X of the depletable multiple-region body portion 10 (i.e. the length of the alternating regions 11 and 12 between the blocking junction 40 and the interface with the drain region 3) is chosen in accordance with the desired blocking capability of the device, which is generally in excess of 100V. The invention becomes even more useful for even higher blocking voltages, for example at least 500V. For a 500V device the thickness X of the region 10 may typically be 50μm. A thickness X of 350μm could be used to make a MOSFET of 4.5kV blocking capability. The balance in net charge (Na.w1 - Nd.w2) of the regions 11 and 12 may be, for example, within ± 10%, and the width w1 of the p-type regions 11 may be in the range 5μm to 10μm.

The bonded junctions 21 between the regions 11 and 12 may be p-n junctions 21a, as illustrated in Figure 4a. However, the present invention permits an alternative to be achieved, having a thin insulating interface layer 21b between the regions 11 and 12. Thus, a thin layer of silicon dioxide may be formed on the major surfaces 100a and 100b of the silicon wafers before the direct bonding step (b). This interface layer 21b of silicon dioxide may be formed on the major surfaces 100a and 100b of alternate wafers, i.e. either the

p-type wafers 110 or the n-type wafers 120, or it may be formed on both wafers 110 and 120. The interface layer 21b is much thinner than the wafers 110 and 120. The conditions for direct bonding of silicon wafers with an oxide interface layer are taught in the two referenced Philips Journal of Research papers. A stronger bond can even be achieved with such an interface. The bonded junctions 21 of the Figure 1 device can comprise such an interface layer 21b as a coupling dielectric between the regions 11 and 12, without adversely affecting the depletion of the regions 11 and 12 by the blocking voltage.

The present invention is particularly useful for manufacturing a vertical device such as Figure 1, in which the respective thicknesses of the wafers 110 and 120 correspond to a desired width w1,w2 for the regions 11,12. However the present invention may be used to form a lateral device, for example devices such as those of Figures 1 and 4 to 12 of US-A-4,754,310. Thus, grooves may be etched through the bonded junctions 21 of the bonded stack 100 from one major surface of an outer wafer of the bonded stack. Electrodes 32 and 33 may then be provided in the grooves for defining through the material a current path that extends parallel to the bonded junctions 21 and parallel to major surfaces of the wafers 110 and 120.

In the embodiment as described above, ingots were sawn and polished to form the wafers 110 and 120, each with a thickness t1, t2 of the order of 10μm. If thinner wafers are required for a particular device, then a different process may be used such as a so-called "smart cut" process.

The "smart cut" process involves the implantation of hydrogen ions (protons) of a well-defined energy through an optically flat, major surface of the silicon wafer. The wafer has the desired doping concentration (Na or Nd) for a region 11 or 12. The energy of the ions is chosen in accordance with the desired penetration depth of the ions in the wafer. The ion dose is typically of the order of 10^{16} to 10^{17} cm^{-2}. The implanted ions form micro-cavities and/or micro-bubbles at the penetration depth.

The implanted surface is then cleaned and directly bonded to a substrate wafer by Van der Waals forces, after which the assembly is heated

to, for example, 500°C to form a cleavage plane in the implanted wafer by the merging together of the micro-cavities and/or micro-bubbles. Thus, the bulk of the implanted wafer is removed to leave the thin surface-adjoining portion (through which the ions were implanted) bonded to the substrate wafer.

The process is then repeated with a silicon wafer of opposite conductivity type, the implanted surface of which is bonded to the thin surface-adjoining portion cleaved from the first wafer. This second wafer has the desired doping concentration (Nd or Na) for a region 12 or 11. By successive repetitions, the multiple-RESURF material can be built up in this manner to produce the bonded body portion 10 and/or the bonded stack illustrated in Figure 3. This process is suitable for producing material in which the thicknesses t1 and t2 (widths w1 and w2) are of the order of 1μm or less.

From reading the present disclosure, other variations and modifications will be apparent to persons skilled in the art. Such variations and modifications may involve equivalent and other features which are already known in the design, manufacture and use of semiconductor devices, and which may be used instead of or in addition to features already described herein. Although Claims have been formulated in this Application to particular combinations of features, it should be understood that the scope of the disclosure of the present invention also includes any novel feature or any novel combination of features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it relates to the same invention as presently claimed in any Claim and whether or not it mitigates any or all of the same technical problems as does the present invention. The Applicants hereby give notice that new Claims may be formulated to any such features and/or combinations of such features during the prosecution of the present Application or of any further Application derived therefrom.

CLAIMS

1. A method of fabricating a depletable multiple-region semiconductor material comprising alternating p-type and n-type regions which provide a voltage-sustaining space-charge zone when depleted, including the steps of:

(a) providing a plurality of semiconductor wafers of p-type conductivity and a plurality of semiconductor wafers of n-type conductivity each having optically flat major surfaces, the wafers comprising respective doping concentrations for the regions of the material and having respective thicknesses between their major surfaces that correspond to a desired dimension for the regions, and

(b) directly bonding alternate p-type and n-type wafers to each other at their major surfaces to provide the depletable multiple-region semiconductor material in the form of a bonded stack having bonded junctions between the p-type and n-type regions.

2. A method as claimed in Claim 1, wherein the wafers are of silicon, and the bonded junctions comprise an interface layer of silicon dioxide that is formed on the major surfaces of at least alternate wafers before the direct bonding step (b).

3. A method as claimed in Claim 1 wherein the bonded junctions are p-n junctions between the alternate wafers.

4. A method as claimed in any one of Claims 1 to 3, wherein the respective thicknesses of the wafers correspond to a desired width for the regions, and the bonded stack is subsequently sliced transverse to the bonded junctions of the p-type and n-type wafers to provide a semiconductor slice for device manufacture.

5. A method of manufacturing a semiconductor device with a slice of the material fabricated by the method of Claim 4, wherein the slice is provided with electrodes for defining through the material a current path that extends parallel to the bonded junctions and transverse to major surfaces of the slice.

6. A method of manufacturing a high voltage MOSFET device with a slice of the material fabricated by the method of Claim 4, wherein source and drain regions are provided at opposite major surfaces of the slice, the source region being separated from the bonded junctions of the space-charge zone by a channel-accommodating body region of opposite conductivity type to the drain region.

7. A method of manufacturing a high voltage semiconductor device with a bonded stack of the material fabricated by a method as claimed in anyone of Claims 1, 2 or 3, wherein grooves are etched through the bonded junctions of the bonded stack from a major surface of an outer wafer of the bonded stack, and electrodes are provided in the grooves for defining through the material a current path that extends parallel to the bonded junctions and parallel to major surfaces of the wafers.

8. A method as claimed in any one of Claims 5, 6 or 7, wherein the locations of the p-type and n-type regions at one major face are identified before providing the source region and channel-accommodating body region adjacent to said one major face, and the source region and channel-accommodating body region are aligned with respect to the p-type and n-type regions at said one major face.

9. A method as claimed in Claim 8, wherein the locations of the p-type and n-type regions at the one major face are identified by lightly etching said one major face in a selective etchant.

10. A semiconductor material comprising alternating p-type and n-type regions, fabricated by a method as claimed in any one of Claims 1 to 4, or a semiconductor device manufactured by a method as claimed in any one of Claims 5 to 9.

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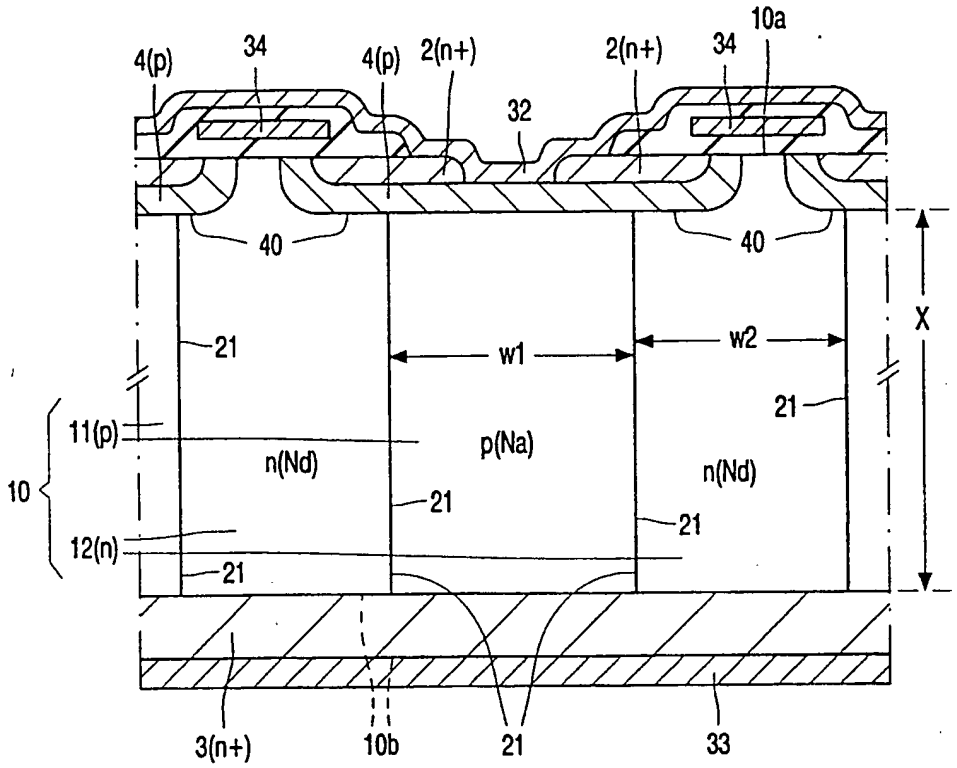
4(p)
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10a
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40
X
21
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w2
21
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10b
21
33

FIG. 1

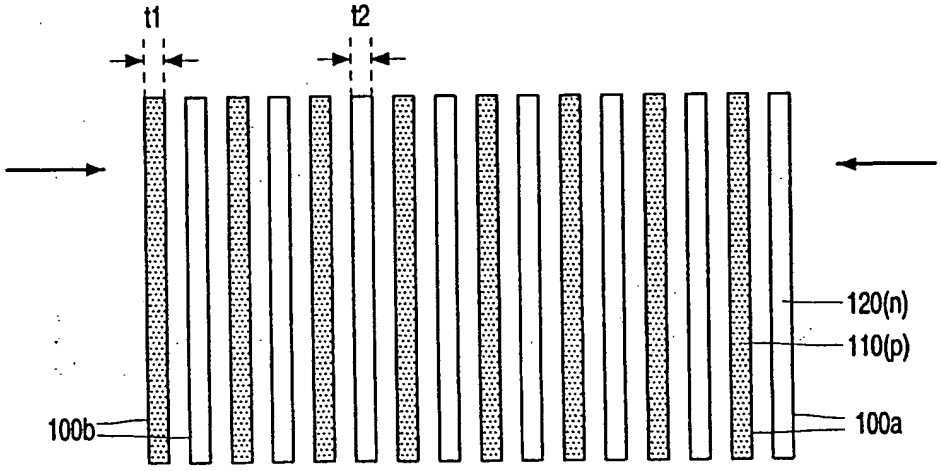
t1
t2
120(n)
110(p)
100b
100a

FIG. 2

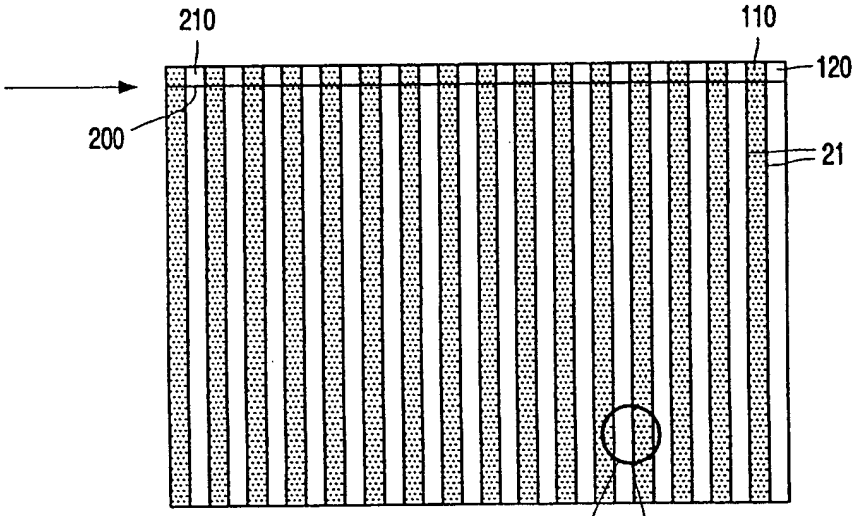

FIG. 3

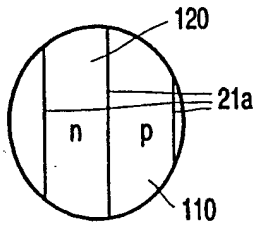

FIG. 4a

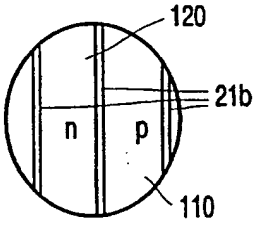

FIG. 4b

INTERNATIONAL SEARCH REPORT

Interr. nal Application No
PCT/EP 00/06332

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/18 H01L21/336 H01L29/06 H01L29/78

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
INSPEC, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 216 275 A (CHEN X) 1 June 1993 (1993-06-01)	10
A	column 5, line 30 -column 6, line 2; figures 2-5 column 1, line 55 -column 3, line 37	1-9
A	HAISMA J ET AL: "SILICON-WAFER FABRICATION AND (POTENTIAL) APPLICATIONS OF DIRECT-BONDED SILICON" PHILIPS JOURNAL OF RESEARCH, vol. 49, no. 1/2, 1995, pages 65-89, XP000508172 BARKING, ESSEX, GB ISSN: 0165-5817 cited in the application figure 3	1

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

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Date of the actual completion of the international search	Date of mailing of the international search report
15 December 2000	02/01/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Morvan, D

1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Intern hal Application No
PCT/EP 00/06332

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5216275 A	01-06-1993	CN 1056018 A	06-11-1991